

REMARKS

In the patent application, claims 1-33 are pending. In the office action, all pending claims are rejected.

Applicant has amended claims 1, 5 - 7, 9 - 19, 24, 25, 26 and 33, and canceled claims 2 and 8.

Applicant has amended claims 1, 5, 6, 7, 9, 10, 11, 12, 14, 16 and 17 to include the limitation that the first electronic module is a host device and the second electronic module is a memory card. The support can be found in Figures 1 and 2. Applicant has amended claims 1, 12, 18 and 24 to include the limitation that the second bit pattern contains at least a part of a reversed pattern of the first bit pattern. The support can be found on p. 6, lines 3 – 15 and p. 7, lines 3-8. Claim 1 also has the limitation of claim 2, which is now canceled.

Applicant has further amended claims 12 – 17 to change the software program to a software application product embedded in a computer readable medium having a plurality of executable coded.

No new matter has been introduced.

At section 2, the Examiner states that the claim objection for the mis-numbered claim 32 has not been overcome. Applicant has renumbered this mis-numbered claim 32 as claim 33.

At section 4, claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Cedar et al.* (WO-02/15020 A2, hereafter referred to as *Cedar*), in view of *Coyle et al.* (U.S. Patent No. 6,473,871, hereafter referred to as *Coyle*).

In rejecting claims 1 and 18, the Examiner states that *Cedar* teaches that a host determines the data bus width of the SD card by reading the information stored in the SD Card Configuration Register (SCR, p.15, last paragraph). The Examiner considers the read command as the first bit pattern and the SCR data as the second bit pattern.

It is respectfully submitted that the second bit pattern, according to the claimed invention, contains at least a part of a reversed pattern of the first bit pattern. *Cedar* does not disclose or suggest that the SCR data contains at least a part of the reversed pattern of the read command.

The Examiner admits that *Cedar* fails to teach that the second bit pattern has a predetermined relationship with a second bit pattern, but points to *Coyle* for teaching such a predetermined relationship.

Coyle discloses a method of testing data errors in transmission, wherein a received pattern is compared to the transmit pattern through a number of test cycles. If the received pattern does not correspond to the transmit pattern, then errors are said to occur in the transmission (col.10, lines 29-38). *Coyle* is concerned with signaling errors due to low signal-to-noise ratios and signal distortion (col.2, lines 62-67). *Coyle* uses a loopback method for error testing wherein the test pattern traverses the bus twice, once in a forward direction and once in the reverse direction during loopback (col.7, lines 48-50). In particular, the pattern in the forward direction is a voltage level sequence or pattern generated by a pattern source 226 in a stimulus cycle and the pattern in the reverse direction is generated by an echo generator 228 in the echo cycle which is a replica version of the stimulus cycle (col.7, lines 53-60). Although *Coyle* mentions a forward pattern signal (signal in the forward direction) and a reverse pattern signal (signal in the reverse direction), *Coyle* does not disclose or suggest that a second bit pattern has at least a part of a reversed pattern of the first bit pattern and that the second bit pattern is compared with the first bit pattern based on a complementary relationship between the first bit pattern and the reversed pattern of the first bit pattern.

For the above reasons, claims 1 and 18 are clearly distinguishable over the cited *Cedar* and *Coyle* references.

In rejecting claim 12, the Examiner states that *Coyle* discloses a bus testing logic 102 which can be implemented in software. However, *Coyle* does not disclose that the second bit pattern contains at least a part of a reversed pattern of the first bit pattern. Furthermore, *Cedar* does not disclose or suggest that the SCR data contains at least a part of the reversed pattern of the read command.

For the above reasons, claim 12 is clearly distinguishable over the cited *Cedar* and *Coyle* references.

In rejecting claims 24 and 25, the Examiner states *Cedar* discloses an electronic device having a first and second bit patterns and *Coyle* discloses a predetermined relationship between the first and second bit pattern. However, *Coyle* does not disclose that the second bit pattern contains at

least a part of a reversed pattern of the first bit pattern. Furthermore, *Cedar* does not disclose or suggest that the SCR data contains at least a part of the reversed pattern of the read command.

For the above reasons, claims 24 and 25 are clearly distinguishable over the cited *Cedar* and *Coyle* references.

In sum, claims 1, 12, 18, 24 and 25 are distinguishable over the cited *Cedar* and *Coyle* references.


As for claims 3-7, 9-11, 13-17, 19-23 and 26-33, they are dependent from claims 1, 12, 18 and 24 and recite features not recited in claims 1, 12, 18 and 24. For reasons regarding claims 1, 12, 18 and 24 above, claims 3-7, 9-11, 13-17, 19-23 and 26-33 are also distinguishable over the cited *Cedar* and *Coyle* references.

CONCLUSION

As amended, claims 1, 3-7 and 9-33 are allowable. Early allowance of these claims is earnestly solicited.

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